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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,140	03/19/2001	Herbert J. Neuhaus	5740.02	7640

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DORSEY & WHITNEY, LLP
INTELLECTUAL PROPERTY DEPARTMENT
370 SEVENTEENTH STREET
SUITE 4700
DENVER, CO 80202-5647

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/812,140	NEUHAUS ET AL.
	Examiner	Art Unit
	Alexander O Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-92* is/are pending in the application.

4a) Of the above claim(s) *1-20,29-47 and 55-92* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-28 and 48-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Serial Number: 09/812140 Attorney's Docket #: 5740.02
Filing Date: 3/19/01;

Applicant: Neuhaus et al.

Examiner: Alexander Williams

Applicant's Amendment in Paper No. 13, filed 4/25/02 is acknowledged.

This application contains claims 1-20, 29-47 and 55-92 drawn to an invention non-elected with traverse in Paper No. 10. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

The disclosure is objected to because of the following informalities: the application related applications should be updated.

Claim 27 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 27, it is unclear and confusing to what is meant by "wherein the substrate comprises a semiconductor chip." It appear that the drawing have both a semiconductor chip and a substrate.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21 to 28, and 48 to 51, insofar as claim 27 can be understood, are rejected under 35 U.S.C. § 102(e) as being anticipated by Estes et al. (U.S. Patent # 6,410,415 B1).

For example, in claim 21, Estes et al. (figures 1 to 8) specifically **figure 6** show an electrical component assembly comprising: a) a substrate **3** having a plurality of electrical contact sites **4** on a surface thereof; and b) a plurality of hard particles **8** positioned on the substrate, such that each of the electrical contact sites has at least one hard particle associated therewith, the hard particles being affixed to the electrical contact sites **(see column 7, line 7 to column 8, line 33)**.

In claim 22, Estes et al.'s plurality of hard particles is affixed to the electrical contact sites by a layer of plated nickel **(see column 5, lines 27-37)**.

In claims 23 and 49, Estes et al. further comprises an non-conductive adhesive material **5** applied to at least selected portions of the surface of the substrate and the plurality of hard particles.

In claims 24 and 50, Estes et al.'s non-conductive adhesive **5** covers substantially all of the substrate **3**.

In claim 25, Estes et al.'s non-conductive adhesive **5** covers selected portions of the substrate **3**.

In claims 26 and 51, Estes et al.'s plurality of hard particles is affixed to the electrical contact sites by plating a thin metal layer over the plurality of hard particles on the electrical contact sites.

In claim 27, Estes et al.'s substrate comprises a semiconductor chip **1**.

In claim 28, Estes et al.'s hard particles are selected from diamond **(see column 7, lines 7-60)**

For example, in claim 48, Estes et al. (figures 1 to 8) specifically **figure 6** show a printed circuit interconnection assembly comprising: a printed circuit board substrate **3** having a plurality of electrical sites **4** on a surface thereof; and a plurality of hard particles **8** positioned on the substrate, such that each of the plurality of electrical contact sites has at least one hard particle associated therewith, wherein the at least one hard particle is affixed to each electrical contact site **(see column 7, line 7 to column 8, line 33)**.

Claims 21 to 27 and 48 to 52 are rejected under 35 U.S.C. § 102(e) as being anticipated by Mase (U.S. Patent # 6,404,476 B1).

For example, in claim 21, Mase (figures 1 to 4) specifically **figure 3** show an electrical component assembly comprising: a) a substrate **1** having a plurality of electrical contact sites **9** on a surface thereof; and b) a plurality of hard particles **7** positioned on the substrate, such that each of the electrical contact sites has at least one hard particle associated therewith, the hard particles being affixed to the electrical contact sites **(see column 3, line 61to column 4, line 21)**.

In claim 22, Mase's plurality of hard particles **7** is affixed to the electrical contact sites by a layer of plated nickel **(see column 3, lines 44-61)**.

In claims 23 and 49, Mase further comprises an non-conductive adhesive material **8** applied to at least selected portions of the surface of the substrate and the plurality of hard particles.

In claims 24 and 50, Mase's non-conductive adhesive **8** covers substantially all of the substrate **1**.

In claim 25, Mase's non-conductive adhesive **8** covers selected portions of the substrate **1**.

In claims 26 and 51, Mase's plurality of hard particles **7** is affixed to the electrical contact sites **9** by plating a thin metal layer over the plurality of hard particles on the electrical contact sites **(see column 3, lines 44-61)**.

In claim 27, Mase's substrate comprises a semiconductor chip **1,2**.

For example, in claim 48, Mase (figures 1 to 4) specifically **figure 3** show a printed circuit interconnection assembly comprising: a printed circuit board substrate **1** having a plurality of electrical sites **9** on a surface thereof; and a plurality of hard particles **7** positioned on the substrate, such that each of the plurality of electrical contact sites has at least one hard particle associated therewith, wherein the at least one hard particle is affixed to each electrical contact site **(see column 3, line 61to column 4, line 21)**..

In claim 52, Mase's printed circuit board substrate **1** comprises a flexible printed circuit board substrate **(see column 1, lines 20-28).**

Claims 21 to 25, 28, and 48 to 50 are rejected under 35 U.S.C. § 102(b) as being anticipated by Zimmer (U.S. Patent # 5,921,856).

For example, in claim 21, Zimmer (figures 1A to 9B) specifically figure 4 show an electrical component assembly comprising: a) a substrate **26** having a plurality of electrical contact sites (inherit) on a surface thereof; and b) a plurality of hard particles **28** positioned on the substrate, such that each of the electrical contact sites has at least one hard particle associated therewith, the hard particles being affixed to the electrical contact sites.

For example, in claim 48, Zimmer (figures 1A to 9B) specifically figure 4 discloses a printed circuit interconnection assembly comprising: a printed circuit board substrate **26** having a plurality of electrical sites (inherit) on a surface thereof; and a plurality of hard particles **28** positioned on the substrate, such that each of the plurality

of electrical contact sites has at least one hard particle associated therewith, wherein the at least one hard particle is affixed to each electrical contact site.

Claims 53 and 54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent # 6,410,415 B1) in view of Herbst (U.S. Patent # 5,913,110).

Estes et al. show the features of the claimed invention as detailed above, but fails to explicitly show wherein the printed circuit board substrate comprises a smart card chip module or a smart label.

Herbst is cited for showing a method for producing a plastic material composite component. Specifically, Herbst (figures 1 to 15) specifically figure 4 discloses wherein the printed circuit board substrate comprises a smart card chip module or a smart label (see column 1, lines 33-65) for the purpose of providing a carrier element having protection for the chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Herbst's smart card chip module or a smart label to modify Estes's substrate for the purpose of providing a carrier element having protection for the chip.

Claims 53 and 54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mase (U.S. Patent # 6,404,476 B1) in view of Herbst (U.S. Patent # 5,913,110).

Mase show the features of the claimed invention as detailed above, but fails to explicitly show wherein the printed circuit board substrate comprises a smart card chip module or a smart label.

Herbst is cited for showing a method for producing a plastic material composite component. Specifically, Herbst (figures 1 to 15) specifically figure 4 discloses wherein the printed circuit board substrate comprises a smart card chip module or a smart label (see column 1, lines 33-65) for the purpose of providing a carrier element having protection for the chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Herbst's smart card chip module or a smart label to modify Mase's substrate for the purpose of providing a carrier element having protection for the chip.

Claims 53 and 54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent # 6,410,415 B1) in view of Oxman et al. (U.S. Patent # 6,395,124 B1).

Estes et al. show the features of the claimed invention as detailed above, but fails to explicitly show wherein the printed circuit board substrate comprises a smart card chip module or a smart label.

Oxman et al. is cited for showing a method for producing a laminated structure. Specifically, Oxman et al.(figures1A to 1D) specifically figure 1D discloses wherein the printed circuit board substrate **14** comprises a smart card chip module or a smart label (see column 9, line 65 to column 10, line 22) for the purpose of providing a carrier element having protection for the chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Oxman et al.'s smart card chip module or a smart label to modify Estes's substrate for the purpose of providing a carrier element having protection for the chip.

Claims 53 and 54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mase (U.S. Patent # 6,404,476 B1) in view of Oxman et al. (U.S. Patent # 6,395,124 B1).

Mase show the features of the claimed invention as detailed above, but fails to explicitly show wherein the printed circuit board substrate comprises a smart card chip module or a smart label.

Oxman et al. is cited for showing a method for producing a laminated structure. Specifically, Oxman et al.(figures1A to 1D) specifically figure 1D discloses wherein the printed circuit board substrate **14** comprises a smart card chip module or a smart label (see column 9, line 65 to column 10, line 22) for the purpose of providing a carrier element having protection for the chip.

Therefore, it would be obvious to one of ordinary skill in the art to use Oxman et al.'s smart card chip module or a smart label to modify Mase's substrate for the purpose of providing a carrier element having protection for the chip.

Response

Applicant's arguments filed 4/25/02 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,779,784,786,787,738,737,734,700,701,758	1/25/02 7/29/02
Other Documentation: foreign patents and literature in 257/778,779,784,786,787,738,737,734,700,701,758	1/25/02 7/29/02
Electronic data base(s): U.S. Patents EAST	1/25/02 7/29/02

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

7/29/02

Primary Examiner
Alexander O. Williams